University of Illinois at Urbana-Champaign **Physics Department**
Digital Electronics Laboratory **Physics 405 Laboratory**

Experiment 1: Analog / Digital Circuits

Contents Page

Revised October, 2004.

1. Introduction

This experiment is an introduction to digital circuits used in conjunction with comparators and analog bilateral (i.e. bipolar) FET switches. We will investigate the behavior and performance properties of analog FET switches, standard comparators, window comparators, Schmitt trigger circuits, Op-Amp to TTL interface circuits and investigate an example of a zero crossing detector and various uses of the 555 Timer IC. Since some of the circuits are simple and straight-forward, you may begin building your circuits on the breadboard directly. Or, if you prefer, try first with *Electronic Workbench* software to simulate these circuits. Make note to use the equivalent IC *4066* model instead of *4016* in your *EWB* simulations.

2. Bilateral (Bipolar) Analog Electronic FET Switch

FET's biased to operate in their variable resistance region are widely used as analog electronic switches. The CMOS *4016B* contains 4 identical bilateral (i.e. bipolar) analog FET switches, each with a separate control line. In order to switch analog signals that can be *either* positive or negative, it is therefore necessary to power the *4016B* chip between ±5 V. In that case, the control line must *also* swing to both supply rails. **Important:** Tie **ALL** unused inputs of the *4016B* chip to either V_{SS} = +5 V or V_{DD} = –5 V and do **NOT** apply voltages to **ANY** of the inputs of the *4016B* chip when the power is off! Spec sheets for the *4016B* chip can be found in the Motorola CMOS or National Semiconductor data books – they are also online on the UIUC P405 web page . Wire up the circuit shown in Figure 1 and simply switch the control line by hand between +5 V and –5 V while applying a bipolar, ~ 1 volt p-p sine wave (output from the Wavetek function generator) to the input of the analog FET switch. Monitor the output sine wave. (a) Measure the FET switche's ON resistance R_{ON} by measuring output voltage as measured using a scope (n.b. which has a 1 Meg Ohm (& 20 pF) input impedance), then lowering the output resistance using a 100 Ohm load resistor (labeled R in Fig. 1 below).

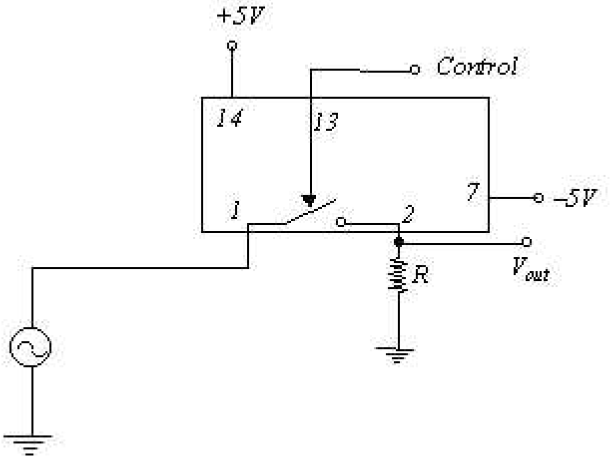

Figure 1. One section of the CMOS *4016B* analog FET switch.

Revised October, 2004.

Draw out the complete circuit diagram in your lab book, including the input impedance of the scope. Measuring V_{out} with and without the load resistor, R, and using e.g. Ohm's law V = IR and Kirchoff's laws, you can solve for the (unknown) ON resistance of the analog FET switch, R_{ON}.

(b) Measure the ratio between output and input, in decibels, when the FET switch is open. Measure this ratio for a few frequencies up to the maximum the function generator can put out. How does this ratio change with load resistance ? Why? {Hint – FET's also have capacitances – are these included in your circuit diagram? What about the scope's 20 pF input capacitance – does this matter?}

Suppose we now want to drive the FET switch from a TTL output. We will need a translator circuit to take the 0-5 V TTL output and turn it into –5 to +5 Volt output. The PNP transistor should do the job nicely. Wire the complete circuit as shown in Figure 2 and drive the TTL input with a unipolar 0-4 V square-wave. Use a pull-down resistor to ground on the output side of the analog switch, as you did in the previous circuit above. Show that the output of the FET is a series of "tone bursts' much like a busy signal on a telephone.

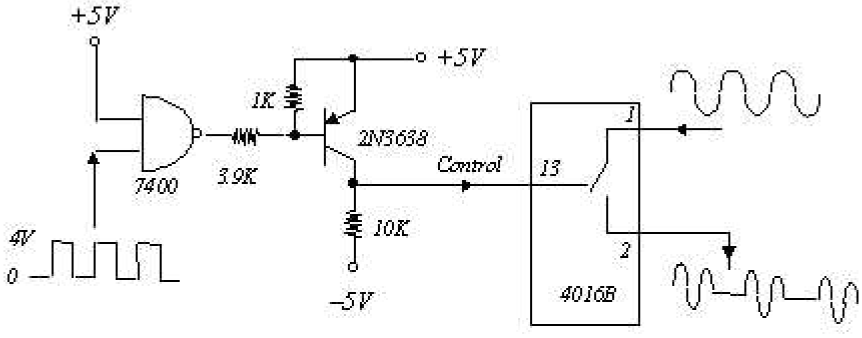

Figure 2. Driving a FET switch from a TTL output.

3. Comparator, Schmitt Trigger

The comparator is a common interface between digital and analog circuitry. The output is high or low depending upon whether the input voltage is above or below a certain level. In principle, any high gain differential amplifier will work, but there are chips optimized for the task, such as the LM339 Quad Comparator. [For example, see Chapter 5, Voltage Comparators, in the *National Semiconductor Linear Databook*,].

As shown in Figure 3, first wire up a LM339 to trigger when the input voltage reaches, say, 2.5 Volts. Power the LM339 with $V_+ = 5$ V, $V_- = -5$ V. Use e.g. 1 μF tantalum (or otherwise) capacitors across the ±5 V power supplies to ground to (locally) suppress spurious, fast transient glitches from the power consumption of the LM339 and/or the 7400 TTL NAND gate. Bypassing the power suppl(ies) in this manner is useful/important to do for any/all digital logic circuits!

Make the LM339 comparator output drive a TTL NAND gate, noting carefully that the output of the LM339 is *open* collector, so you will need a pull-up resistor, e.g 1-2 KΩ on the output of the LM339. Next, add hysteresis to the comparator. This new circuit, called a Schmitt trigger, gives clean transitions even when the input has substantial noise. Measure the amount of hysteresis. The easiest way to do this is to drive the input with a sine wave and look at the TTL transitions simultaneously on the scope. Hysteresis should be used whenever possible since the rapid transitions in logic circuits can cause noise spikes on the ground line. These noise spikes can inadvertently trigger a comparator without hysteresis.

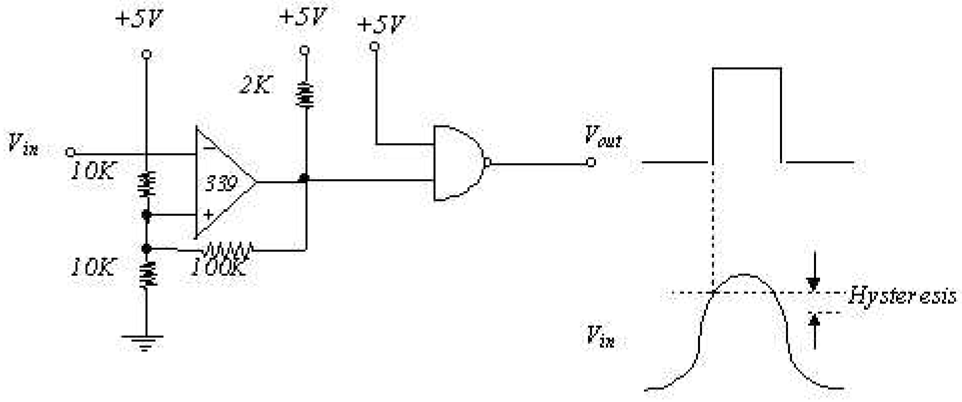

Figure 3. Schmitt trigger circuit with LM339 quad comparator.

4. Op Amp to TTL Interface, Zero Crossing Detector

It is sometimes necessary to interface an ordinary op amp to a logic circuit input. Since op amps do not have open collector outputs, a somewhat different arrangement is necessary, as shown in Figure 4. The diode protects the base-emitter junction of the transistor (which is either off or saturated, depending upon the op-amp output). The op amp is wired to produce a "zero crossing detector" with some hysteresis. Measure the time delay between an input sine wave zero crossing and the TTL output transition. By looking at the op amp output, show that this delay is related to the finite slew rate of the op amp.

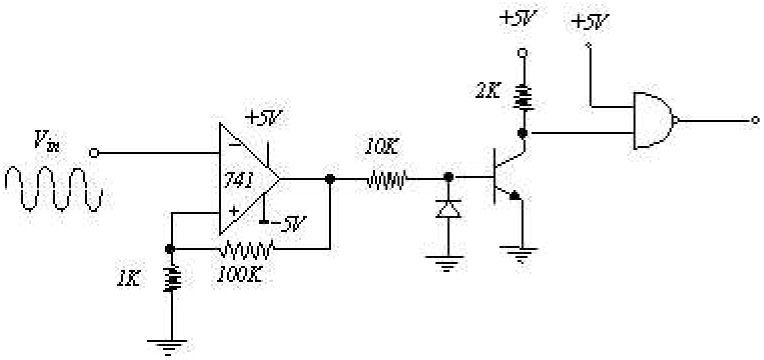

Figure 4. Zero crossing detector circuit.

5. Window Comparator

Next, build the "window comparator" shown in Figure 5. Explain how it works. A window comparator is useful in particle spectroscopy where we want to count only voltage pulses whose peak height lies within a narrow range. Drive it with a sine wave and demonstrate how the output triggers only when the sine wave is within a window of voltage. Since the 339 outputs are open collector, it is possible to wire them together. You can't do this with conventional op amps ! Because of the fast response times of the ICs, it is strongly recommended to add e.g. ~ 20-50 μF tantalum capacitors .and. e.g. 0.1μF capacitors on the ±5V power supply lines on your breadboad, in order to prevent oscillations. Note that the tantalum capacitors are polarized! You may e.g. additionally need to bypass the voltage divider resistor with, say, 100 pF to avoid oscillations.

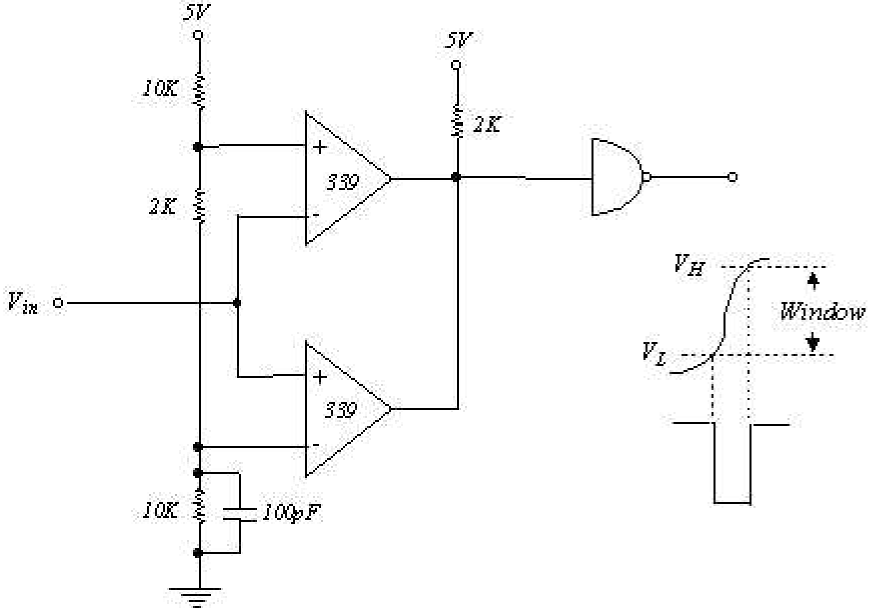

Figure 5. Op-Amp Window Comparator.

6. <u>555 Timer Chip</u>

The 555 is one of the most popular integrated circuits of all time. It is essentially a relaxation oscillator employing a combination of analog and digital circuitry. Its operation is described in many electronic textbooks (for example, see *The Art of Electronics* by *Horowitz and Hill* or *Microelectronic Circuits* by *Sedra and Smith*).

The 555 is a complex chip used in many applications as an astable free running clock or monostable pulse generator. The 555 Timer IC is very easy to use, powered by +5V, works/interfaces directly with TTL logic. The 555 Time needs only an external capacitor and two resistors in order to work e.g. as an astable multivibrator. A block diagram of the 555 Timer is shown below in Figure 6.

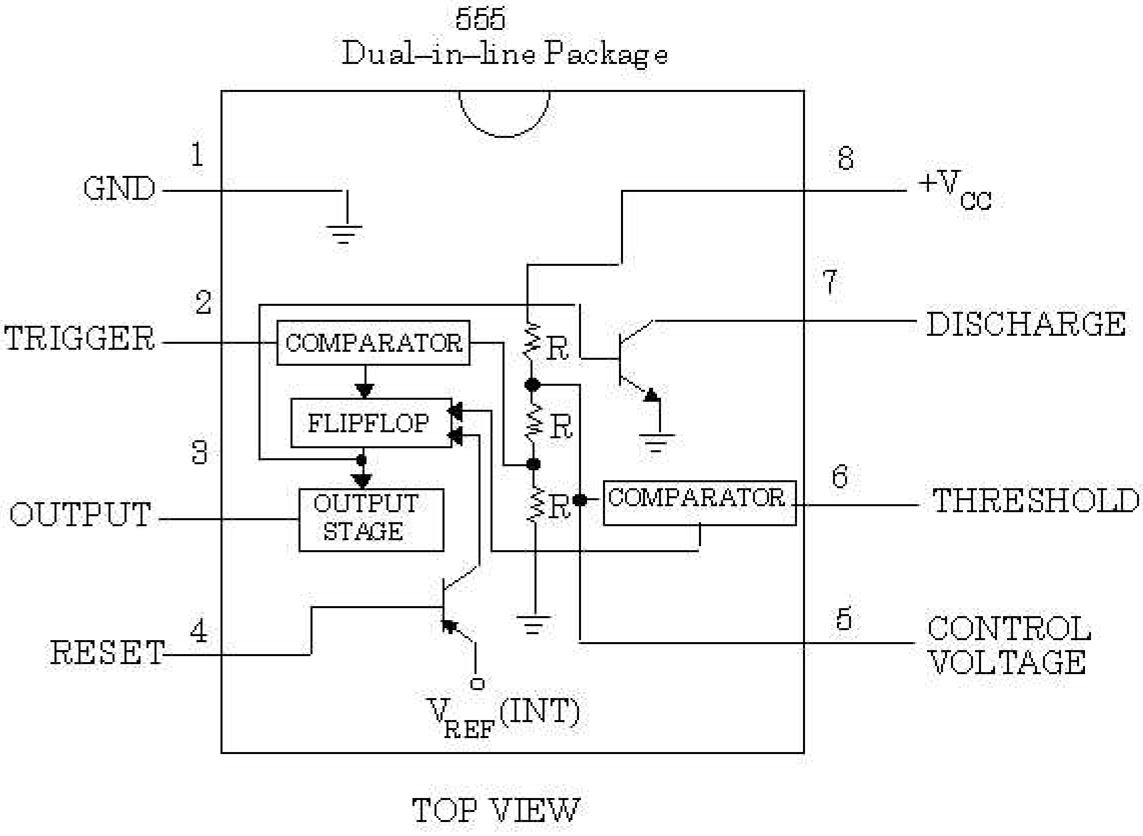

Figure 6. Block diagram of 555 Timer.

The timing capacitor, C that is used in the 555 Timer circuits always has one end connected to ground, and the other end to a positive voltage, thus permitting e.g. the use of electrolytic capacitors for very long timing periods.

The circuit for a 50% duty cycle oscillator using the 555 Timer IC is shown in Fig. 7.

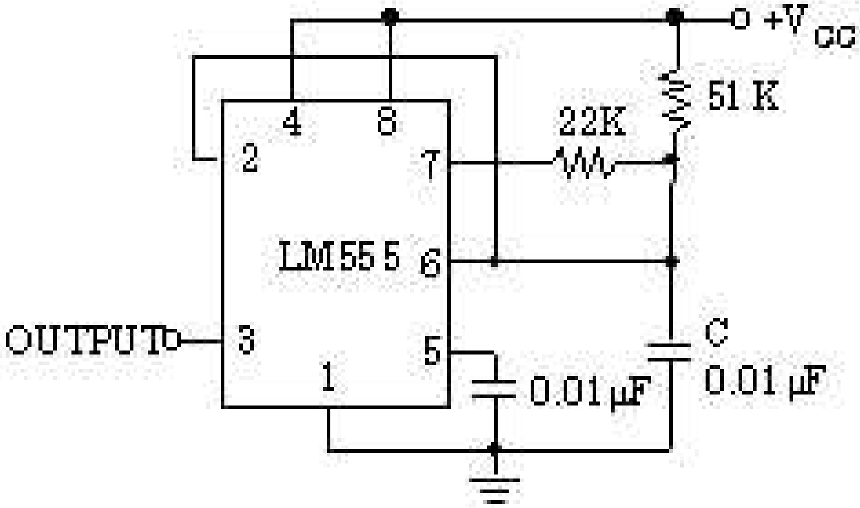

Figure 7. 50% Duty Cycle Oscillator with 555 Timer.

The use of the 555 Timer IC for an astable multivibrator circuit is shown in Fig. 8.

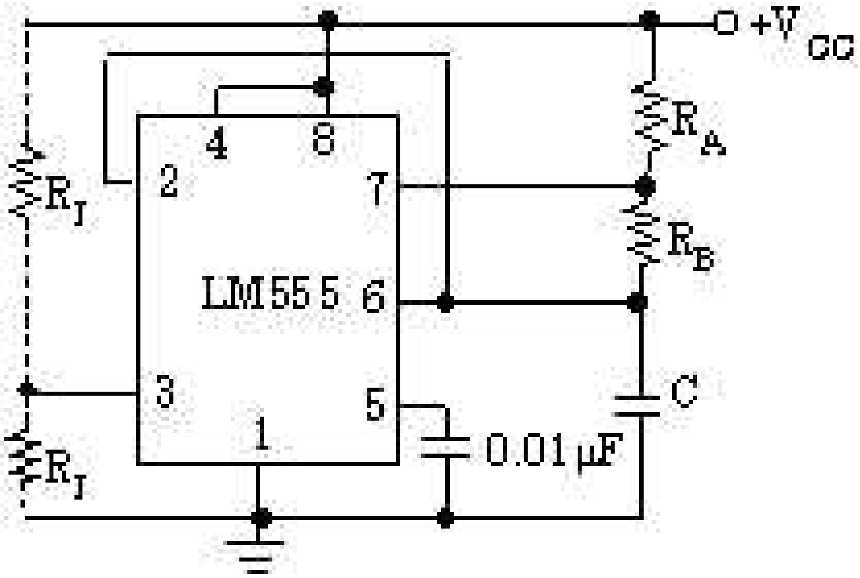

Figure 8. Astable Multivibrator circuit using the 555 Timer IC.

The graph shown in Fig. 9 indicates how to determine the values of external components, C, R_A and R_B in order to achieve the desired (so-called “free-running”) frequency of operation for the astable multivibrator.

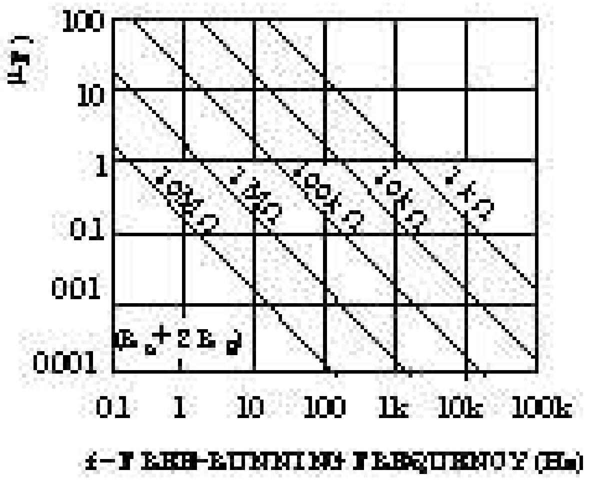

Figure 9. Free running frequency graph for astable multivibrator 555 Timer.

The duty cycle, D for the output associated with the use of the 555 Timer IC as an astable multivibrator, for D ≤ 50% is given by

$$D = \frac{R_B}{R_A + 2R_B}$$

Note this formula implies that for a 50% duty cycle, i.e. $D = 0.5$, that $R_A = 0$. If the value of R_B is large with respect to R_A, then a ~ 50% duty cycle, i.e. a ~ symmetrical unipolar square wave is output from the 555 Timer. For a duty cycle > 50%, the duty cycle formula is

$$D_{l\arg e} = \frac{R_A + R_B}{R_A + 2R_B}$$

Figure 10 shows the circuit for the 555 Timer configured as a monostable multivibrator.

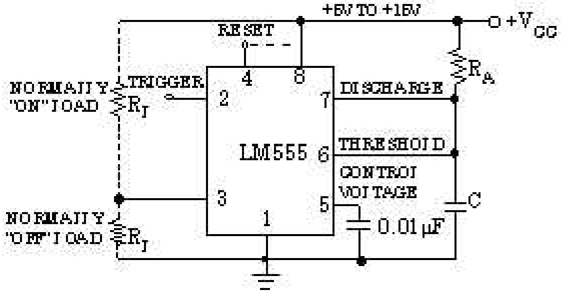

Figure 10. Monostable multivibrator circuit using the 555 Timer.

Figure 11 shows the graph needed for determining the values of external components *C* and R_A for a particular choice of time delay for the 555 monostable multivibrator.

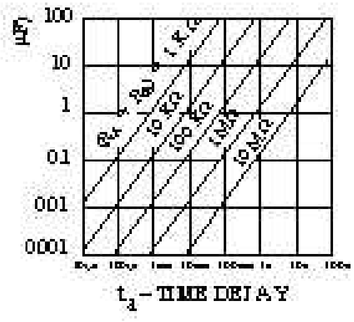

Figure 11. Time Delays for various R_A and *C* values for the 555 monostable multivibrator.

<u>Build an Astable Multivibrator using the 555 Timer IC:</u>

a.) Construct an astable multivibrator circuit using the 555 Timer IC for a *D* = 50% duty cycle/symmetrical, unipolar output at a free running frequency of f = 1 KHz. Use +5 V power supply to power this circuit. Note that the free-running frequency is given by:

$$f_{free-running} = \frac{1.44}{(R_A + 2R_B)C}$$

with resistances R_A and R_B in Ohms and capacitance, *C* in Farads:

b.) Modify the above circuit in order to obtain a duty cycle of *D* = 10%. Refer to Figs. 8 and 9 above.

c.) Is the free-running frequency modified/altered by increasing the power supply from 5 to 15 volts in case b.) above?

Build a Monostable Multivibrator uing the 55 Timer IC:

The 555 timer chip can be configured as a pulse generator as shown in Fig. 10 (monostable multivibrator configuration). An external, unipolar square wave-type pulse applied to the input pin 2 of the 555 Timer IC triggers a unipolar square wave-type output pulse from this circuit. The duration of the output pulse is determined by the value of R_A and C as shown in the Fig. 11. The reset input pin 4 can be used to inhibit the monostable action or to stop a timing cycle after it begins.

a) Construct a 555 Timer IC-based monostable multivibrator circuit with an output pulse width of 5 ms. Note that the period of the monostable multivibrator circuit is $T = 2.2R_AC$, therefore the pulse width, for a 50% duty cycle is $T/2 = 1.1R_AC$. Connect a $f = 1$ KHz, $D < 50\%$ (i.e. asymmetric) unipolar square wave-type pulse from the Wavetek function generator to the trigger input (pin 2) of the 555 Timer IC.

b) Is the output pulse of the 555 timer monostable multivibrator triggered by the rising or the falling ***edge*** of the unipolar input trigger pulse, or is it triggered by the logic 0 or logic 1 ***level*** of the unipolar input trigger pulse?

c) What is the minimum amplitude of the unipolar input trigger pulse?