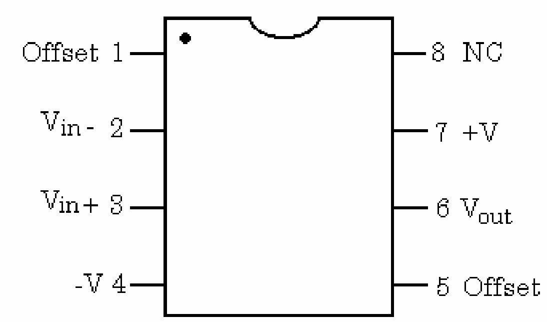
Lab 3 — Operational Amplifiers

In this lab we will learn characteristics of operational amplifiers and their use in simple configurations.

Section A ---- Operational Amplifier Characteristics

The following shows the connection to a 741 op-amp, viewed from top.

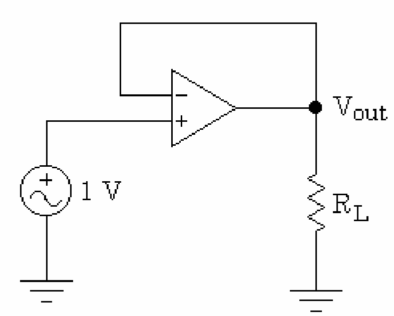


In general, ideal op-amps obey the *Golden Rules*:
- Infinite input impedance (actually about 1MΩ)
- Zero output impedance (actually about a few 10's of Ohms)
- Infinite differential mode gain (about 100,000 at 10Hz, falls of at –20dB/dec)
- Zero common mode gain

Op-amps are usually wired with (negative) feedback so that the response of the system is dependent on external components and not as much on the op-amp. The gain is then controlled by how much of the output is fed back into the input.

When designing circuits with op-amps there are a few simplifying assumptions that are used: no current flows in or out of the inputs and the op-amp adjusts its output in whatever way necessary to make the voltages at the inputs equal.

Non-Inverting Configuration



1) Construct the circuit above using a 741 op-amp a with R_L=1kΩ. The ±15V power connections are not shown in the schematic, but are definitely needed!

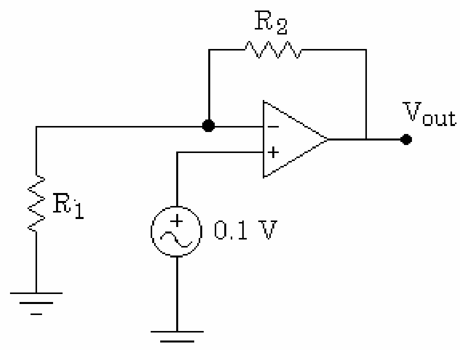
2) Measure the gain as a function of frequency (100, 500, 1k, 5k, 10k, 50k, 100k, 500k, 1M). Remember the DMM can only measure voltages up to 300kHz.

3) At what frequency (f_t) does the gain drop to –3dB?

4) Look at the output wave for R_L = 1k, 500 100, 50, 22 Ohms.

5) For which load do you see distortion in the output? What conclusion can you make about the output current limit of the op-amp?

6) Determine the gain for the 'non-inverting amplifier' circuit shown below.



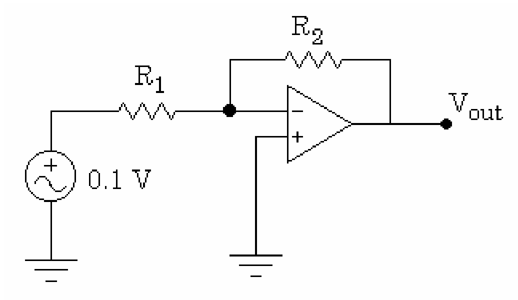
7) Select R_1 and R_2 to give you a gain of 20 and add them to the feedback network of your circuit.

8) Find the frequency where the gain is reduced by 3dB. It is important to remember that the low frquency gain is 20 (i.e. 26dB). You are looking for the frequency where the gain drops to 23dB.

9) Is this the frequency consistent with the information obtained in part 2?

Section B — Inverting Configuration

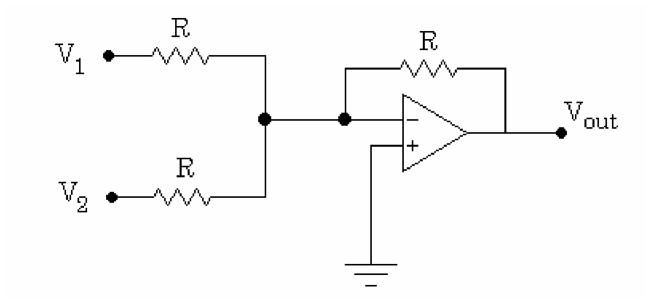
Inverting Amplifier



1) Determine the gain of this amplifier.

2) Construct the circuit above choosing R_1 and R_2 to give you a gain of –100. At what frequency is the gain attenuated –3dB?

Summing Amplifier

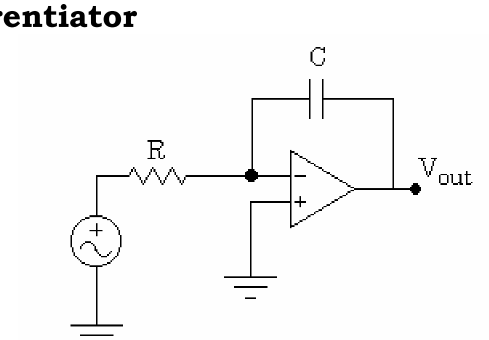


1) Determine how V_{out} relates to V_1 and V_2.

2) Set V_1 = 1V at 1kHz and V_2 = 3.5V DC. Is the output what you expect?

3) Add another op-amp circuit that has a gain of –1 to invert the output from the circuit above and verify the AC and DC components of the output.

Integrator and Differentiator



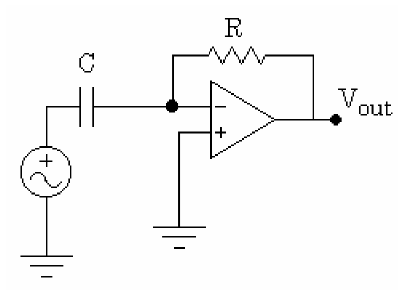
1) Show that output of this amplifier is proportional the integral of the input.

2) Select R and C so that when $\omega=2\pi*10{,}000$ the gain is 1 (i.e. 0dB).

3) Perform an AC analysis of this circuit in EWB.

4) Construct the circuit and input a SQUARE wave from the Wavetek. Add a 10MΩ resistor across the capacitor. Look at the output wave form at frequencies of 100Hz, 10kHz, and 100kHz. Adjust the input voltage so that the output amplitude is < 10V. Sketch, or record a picture with the 'scope camera at the different frequencies.

5) Does the behavior of the circuit match the theory?



6) Repeat for the differentiator shown above. Use the TRIANGLE wave function instead of the SQUARE.

Section C — Op-Amp Limitations

Slew Rate

1) Wire an op-amp in the inverting configuration for a gain of –10.

2) Apply an input signal so that the output voltage is large, about 20Vp-p.

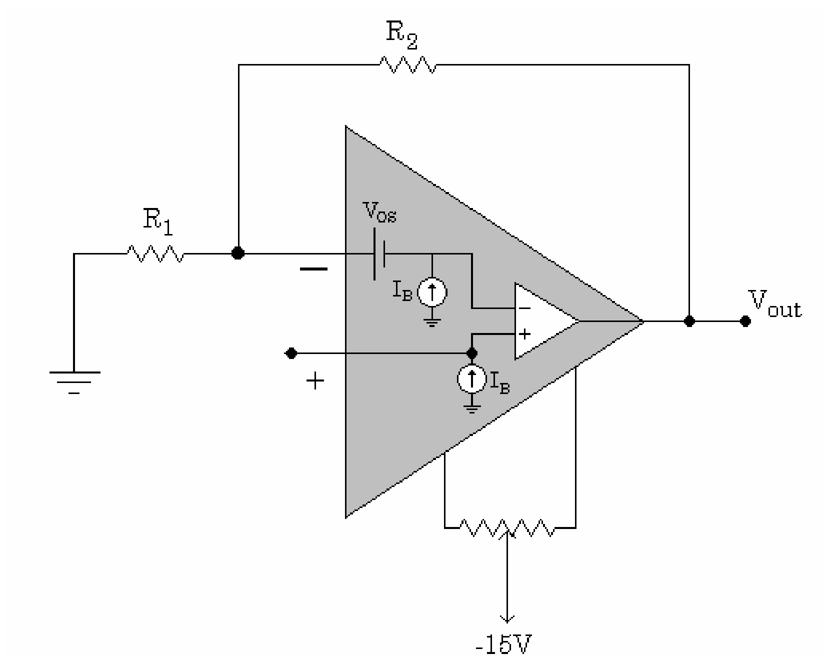
3) Increase the frequency until you see clear signs of slew-rate limiting. This can be seen best when the output becomes a triangle waveform.

4) What is the slew rate of the amplifier?

Input Offset Voltage and Input Bias Current

So far we have considered an op-amp to be ideal. However, there is usually an offset voltage, V_{os}, at the input which can cause problems for high gain circuits. Op-amps also have an input bias current which can produce extra voltages at the inputs due to resistance at the input terminals. Using the offset terminals we can remove this offset.

The model for the non-ideal op-amp is shown below.



1) Choose R_1 and R_2 for a gain of 1,000.

2) Connect a resistor from the positive terminal to ground to eliminate the effect of I_B or make the voltage at the inputs due to I_B the same for both.

3) Measure V_{out}.

4) The output is due to V_{os} since we have removed the effect of I_B. Calculate V_{os} (at the input) using the known gain of the amplifier.

5) Use a 10k potentiometer (pot) and connect it to terminals 1, 5, and –15V as shown. The middle pin of the potentiometer (the wiper) is the one that goes to the –15V supply.

6) Adjust the potentiometer until the output voltage is zero. This removes the effect of V_{os}.

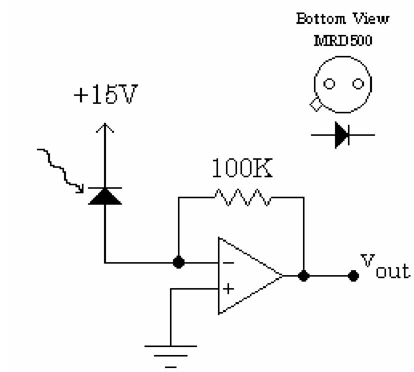
7) Now replace your resistor between the positive (non-inverting) input and ground with 100k and calculate I_B from the output voltage.

8) The circuit used as the input stage of the op-amp is a differential transistor circuit. Considering this information, what causes V_{os} and I_B and how are they eliminated by adjusting the external offset?

Section D — Selected Op-Amp Applications

Current to Voltage Converter

Some devices give a current as the output. One of these is a photodiode. The photodiode produces a current proportional to the amount of light shining on its surface. An op-amp can be used to convert this current to a voltage.



1) Wire the circuit shown above. Look at the output on the oscilloscope.

2) What is the frequency of the observed signal and what is the source of this signal?

3) Add a capacitor in parallel with the resistor to filter out this AC signal and observe the remaining DC voltage output as you vary the illumination of the photodiode.

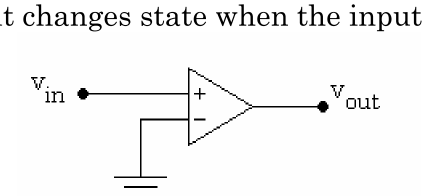
Comparator

An op-amp can also be used as a comparator. A comparator's output is a high level or low level depending upon whether or not the input is greater or less than a threshold voltage.

1) Build the zero crossing detector (comparator circuit) shown below.

2) Look at the input (1 V AC @ 100Hz) and output on the scope.

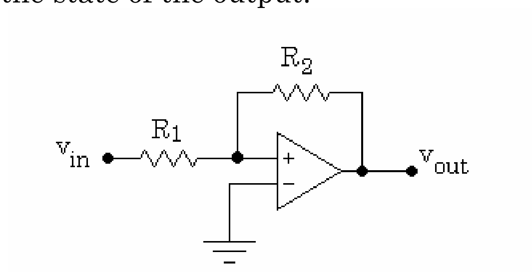
3) Verify that the output changes state when the input crosses zero.



4) To compare an input with a threshold voltage other than zero, one applies the desired threshold voltage to the inverting input of the op-amp. You can demonstrate this by varying the DC offset of the signal generator.

Hysteresis

A comparator can be adversely affected by the presence of noise mixed in with its input signal. When the voltage gets close to the threshold voltage, the output of a comparator can make many transitions. Typically we want only one transition at the output when the input first crosses the threshold. This is very important if the output is going to provide a level for digital logic. To remove the effect of the noise we add positive feedback to introduce *hysteresis* to the circuit. Hysteresis provides a memory of the transition and therefore shifts the threshold voltage according to the state of the output.



1) Determine the low-to-high threshold voltage, V_{TH}, and the high-to-low threshold voltage, V_{TL}. First, assume that the output voltage is in the low state (–15V) and determine what input voltage makes the voltage at V_+ become zero. This is V_{TH}. Then by assuming the output is high (+15V) you can use the same idea to determine V_{TL}.

2) Determine the amount of hysteresis in terms of R_1 and R_2 and choose R_1 and R_2 to give you 1V of hysteresis. The hystersis is defined as $V_{TH} - V_{TL}$.

3) Apply an input voltage of 1V AC @ 100Hz.

4) Measure V_{TH} and V_{TL}, and determine the amount of hysteresis. Does this agree with your design?